AMENDMENTS TO THE CLAIMS:

Claims 1 - 2. (Canceled without prejudice or disclaimer).

3. (Previously Presented) A semiconductor device including a semiconductor substrate, a gate electrode and a plurality of transistors formed on the semiconductor substrate, the plurality of transistors being disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistors and plurality of p-channel field-effect transistors,

the insulating film including tensile stress,

the insulating film that is formed in regions at the peripheries of the p-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain including an insulating film that is thinner than the insulating film that is formed in regions at the peripheries of the n-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain.

4. (original) The semiconductor device of claim 3, further including an interlayer insulating film including an upper end above the insulating film and a wiring layer above the interlayer insulating film.

5. (Previously Presented) A semiconductor device including a semiconductor substrate, a plurality of active regions enclosed by field regions formed on the semiconductor substrate, a gate electrode and a plurality of transistors

formed on the active regions, the plurality of transistors being disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistors and a plurality of p-channel field-effect transistors corresponding to the n-channel field-effect transistors,

the insulating film including tensile stress,

wherein the insulating film that is thinner than the insulating film formed at regions positioned between the first n-channel field-effect transistors and the second n-channel field-effect transistors is formed on, or not disposed on, field regions adjacent to the active regions formed by the p-channel field-effect transistors.

6. (Previously Presented) A semiconductor device including n-channel field-effect transistors and p-channel field-effect transistors formed on a silicon substrate,

wherein the n-channel field-effect transistors and the p-channel field-effect transistors are plurally included,

a direction in which drain currents of the transistors mainly flow is a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

an insulating film including tensile stress is formed at upper portions of the n-channel field-effect transistors and the p-channel field-effect transistors, and

the insulating film that is thinner than the insulating film formed at regions positioned between first n-channel field-effect transistors and second n-

channel field-effect transistors is formed on or not disposed on field regions adjacent the active regions of the p-channel field-effect transistors.

7. (Previously Presented) A semiconductor device including a semiconductor substrate, a gate electrode and a plurality of transistors formed on the semiconductor substrate, the plurality of transistors being disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistors and a plurality of p-channel field-effect transistors,

the insulating film including compression stress,

the insulating film that is formed in regions at the peripheries of the n-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain including an insulating film that is thinner than the insulating film that is formed in regions at the peripheries of the p-channel field-effect transistors and positioned in directions parallel and orthogonal to the direction joining the source and the drain.

8. (Previously Presented) A semiconductor device including a semiconductor substrate, a plurality of active regions enclosed by field regions formed on the semiconductor substrate, a gate electrode and a plurality of transistors formed on the active regions, the plurality of transistors being disposed with a drain and a source corresponding to the gate electrode, an insulating film formed above the transistors, with a direction joining the source and the corresponding drain of the

transistors being formed in a direction along a <100> crystal axis or an axis equivalent to the <100> crystal axis,

the transistors including a plurality of n-channel field-effect transistors and a plurality of p-channel field-effect transistors,

the insulating film including compression stress,

wherein the insulating film that is thinner than the insulating film formed at regions positioned between first p-channel field-effect transistors and second p-channel field-effect transistors is formed on, or not disposed on, field regions adjacent to the active regions of the n-channel field-effect transistors.

9. (Previously Presented) A semiconductor device including a plurality of active regions enclosed by field regions formed on a silicon substrate and n-channel field-effect transistors and p-channel field-effect transistors formed in the active regions,

wherein the n-channel field-effect transistors and the p-channel field-effect transistors are plurally included,

a direction in which drain currents of the transistors mainly flow is a direction along a <100> crystal axis, or an axis equivalent to the <100> crystal axis, an insulating film including compression stress is formed at upper portions of the n-channel field-effect transistors and the p-channel field-effect transistors, and

the insulating film that is thinner than the insulating film formed at regions positioned between first p-channel field-effect transistors and second p-channel field-effect transistors is formed on, or not disposed on, field regions adjacent to active regions of the n-channel field-effect transistors.

Claims 10-16 (Canceled without prejudice or disclaimer).